

**Code No: C0509****JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD****M. Tech I Semester Examinations March/April-2011****ADVANCED COMPUTER ARCHITECTURE****(COMPUTER SCIENCE)****Time: 3hours****Max.Marks:60****Answer any five questions****All questions carry equal marks**

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- 1.a) Explain Amdahl's law.  
b) Explain various addressing modes. [12]
2. Explain the classic five-state pipeline for a RISC processor. [12]
- 3.a) Explain the first miss penalty reduction technique in multilevel caches.  
b) Given the data below, what is the impact of second-level cache associativity on its miss penalty?  
▪ Hit time  $L_2$  for direct mapped = 10 clock cycles.  
▪ Two-way set associativity increases hit time by 0.1 clock cycles to 10.1 clock cycles.  
▪ Local miss rate  $L_2$  for direct mapped = 25%  
▪ Local miss rate  $L_2$  for two-way set associative = 20%  
▪ Miss penalty  $L_2 = 100$  clock cycles. [12]
- 4.a) Explain instruction-level parallelism.  
b) Explain dynamic scheduling with example. [12]
5. Explain pipeline scheduling and loop unrolling. [12]
- 6.a) Explain directory-based cache coherence protocols.  
b) Explain the performance of distributed shared-memory multi processors. [12]
- 7.a) Explain about ATM, wide area network.  
b) Explain the designing procedure of a cluster. [12]
- 8.a) Explain the Intel IA-64 instruction set architecture.  
b) Explain the practical issues in interconnecting networks. [12]

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